AMENDMENTS TO THE CLAIMS

Please amend the claims follows:

1. (Currently Amended) A communication device, comprising:

a central processing unit electrically connected to A address lines and M data lines of a processor bus, wherein the A address lines convey A bits of an address in parallel and the M data lines convey M bits of data in parallel;

~~a signal modulator/demodulator, for effecting radio communications, having an interface operatively connected to a~~ a packet bus having:

control lines for conveying control signals; and

N bidirectional data lines for conveying ~~packetized~~ a command packet~~control~~ and for conveying a data ~~signals~~packet including the M bits of data, wherein each of A and M is greater than N, and wherein A, M and N are integers; and

~~a central processing unit operatively connected to a processor bus including address lines and M data lines, wherein M is greater than N;~~

~~and~~ a master controller, ~~operatively~~ electrically connected to the A address lines and M data lines of the processor bus and to the control lines and the N bidirectional data lines of the packet bus, for controlling via the packet bus a plurality of peripherals ~~operatively~~ electrically connected to the control lines and the N bidirectional data lines of the packet bus.

2. (Currently Amended) The device of claim 1, wherein the master controller includes packet generator configured to packetize the M bits of data ~~signals~~ received in parallel through the M data lines of the processor bus, the ~~packetized~~ M bits of data ~~signals~~ being thereby formatted to be conveyed via the N bidirectional data lines of the packet bus.

3. (Currently Amended) The device of claim 2, further comprising:

a signal modulator/demodulator, for effecting radio communications, having an interface operatively connected to a memory shared by the modem and by the central processing unit, wherein the memory is operatively connected to and on the packet bus and not directly connected to the processor bus~~, shared by the modem and by the central processing unit~~.

4. (Currently Amended) The device of claim 1, wherein the plurality of peripherals operatively connected to and on the packet bus includes a memory shared by the central processing unit and by a~~the~~ signal modulator/demodulator for effecting radio communications, and at least one of an image capture module, a display, and a flash memory.

5. (Currently Amended) The device of claim 1, wherein the master controller controls the plurality of peripherals by issuing a ~~packetized~~ command packet commonly receivable by the plurality of peripherals over the N bidirectional data lines of the packet bus, wherein the ~~packetized~~ command packet includes a module device select signal ~~used~~ for selecting one among the plurality of peripherals.

6. (Currently Amended) The device of claim 5, wherein the selected one of the plurality of peripherals returns a signal to the master controller to acknowledge receipt of the ~~packetized~~ command packet.

7. (Currently Amended) The device of claim 5, wherein the ~~packetized~~ command packet includes:

a read/write command directed to a memory shared by the modem and the central processing unit;

a field that specifies the length of a data packet; and

a field that indicates the start address of the commanded data read/write.

8. (Currently Amended) The device of claim 7, wherein data read from the shared memory is sent to the central processing unit with a strobe signal, the strobe signal is ~~used~~ for strobing the data read into a register in the master controller.

9. (Currently Amended) The device of claim 3, wherein the control lines of the packet bus include:

a first signal line for conveying a first control signal that indicates that the N bidirectional data lines currently carry a command packet or a data packet; and

a second signal line for conveying a second control signal that indicates the current transfer direction over the N bidirectional data lines; and

a forward clock line for conveying a control signal for synchronizing write-data packets.

~~signal modulator/demodulator includes a digital signal processor.~~

10. (Currently Amended) The device of claim 3, wherein the shared memory includes a protection circuit for receiving address data from the central processing unit and the signal modulator/demodulator and for generating a protect signal upon simultaneously receiving the same address from the signal modulator/demodulator and the central processing unit, wherein the protect signal is generated to halt memory access by one of the signal modulator/demodulator and the central processing unit in order to prevent simultaneous access of the same memory cells by both of the signal modulator/demodulator and the central processing unit.

11. (Currently Amended) A communication device, comprising:

a central processing unit operatively connected to A address lines and M data lines of a processor bus, wherein the A address lines convey A bits of an address in parallel and the M data lines convey M bits of data in parallel;

a signal modulator/demodulator, for effecting radio communications~~, having an interface operatively connected to~~

a memory shared by the modulator/demodulator and by the central processing unit;

a first packet bus having:

control lines for conveying control signals; and

N bidirectional data lines for conveying a command packet and for conveying data packets including the M bits of data, wherein each of A and M is greater than N, and wherein A, M and N are integers;

a second packet bus having control lines and N data lines for conveying ~~packetized~~ a command packet~~control~~ and a data ~~signals~~packet including the M bits of data; and

~~a central processing unit operatively connected to a processor bus including address lines and M data lines, wherein M is greater than N; and~~

a first master controller, ~~operatively~~ electrically connected to A address lines and M data lines of the processor bus and to the control lines and N bidirectional data lines of a first packet bus ~~having N data lines~~ for controlling via the first packet bus at least one peripheral on the first packet bus; and

a second master controller, electrically connected to the control lines and N bidirectional data lines of the second packet bus, for controlling ~~via the first packet bus at least one peripheral and~~ via the second packet bus ~~a~~ the memory shared by the modulator/demodulator~~modem~~ and by the central processing unit.

12. (Currently Amended) The device of claim 11, wherein the second master controller is electrically connected to the A address lines and M data lines of the processor bus and further controls ~~via the second bus a~~ flash memory via the control lines and N bidirectional data lines of the second packet bus.

13. (Currently Amended) The device of claim 11, wherein the at least one peripheral on the first packet bus is an image capture module.

14. (Currently Amended) The device of claim 11, wherein the first master controller is configured to controls a plurality of peripherals operatively connected to the first packet bus by issuing a ~~packetized~~ command packet commonly receivable by the plurality of peripherals over the N bidirectional data lines of the first packet bus, and the ~~packetized~~ command packet includes a module device select signal ~~used~~ for selecting one of the peripherals.

15. (Currently Amended) The device of claim 14, wherein the selected one of the plurality of peripherals returns a signal over the control lines of the first packet bus to the first master controller to acknowledge receipt of the command packet.

16. (Currently Amended) The device of claim 14, wherein ~~the~~a ~~packetized~~ command packet directed to the memory shared by the modem and the central processing unit includes:

a field specifying a Read Transfer or a Write Transfer~~a read/write command to the memory shared by the modem and the central processing unit~~;

a field that specifies the length of a data packet; and

a field that indicates the start address of the requested transfer.

17. (Currently Amended) The device of claim 16, wherein data read from the shared memory is transmitted~~sent~~ to the first master controller with a strobe signal, the strobe signal ~~is used~~ for strobing the data read into a register in the first master controller.

18. (Currently Amended) The device of claim 11, wherein M is an integer multiple of N~~the shared memory is an SDRAM~~.

19. (Currently Amended) The device of claim 18, wherein N is four~~the SDRAM includes a plurality of data banks and an interface for interfacing the master controller via the second packet bus~~.

20. (Currently Amended) The device of claim 18, wherein the control lines of the first packet bus include:

a signal line that indicates whether the N bidirectional data lines currently carry a command packet or a data packet;

a signal line that indicates the current transfer direction over the N bidirectional data lines.

~~the SDRAM includes a protection circuit for receiving address data from the central processing unit and the modem via the second packet bus and for generating a protect signal upon simultaneously receiving the same address from the modem and the central processing unit.~~

21. (Currently Amended) An application processor (AP), for use in a communication device, comprising:

a central processing unit, operatively connected to a processor bus including A address lines and M data lines, for processing data received from a plurality of peripherals~~ including a signal modulator/demodulator (modem) for effecting radio communications~~, wherein the A address lines convey A bits of an address in parallel and the M data lines convey M bits of data in parallel; and

a first master controller ~~operatively~~ electrically connected to the M data lines of the processor bus and to the N bidirectional data lines of a first~~second~~ packet bus~~ having N data lines~~, for controlling via the first ~~second~~ packet bus ~~the~~ a plurality of peripherals~~, wherein M is greater than N~~;

wherein the first packet bus includes:

control lines for conveying control signals; and

N bidirectional data lines for conveying a command packet and for conveying a data packet including the M bits of data, wherein each of A and M is greater than N, and wherein A, M and N are integers.

22. (Currently Amended) The device of claim 21, wherein the plurality of peripherals includes a signal modulator/demodulator (modem) for effecting radio communications, and ~~further including a~~ memory ~~operatively~~ electrically connected to N bidirectional data lines of the first packet~~second~~ bus~~, the memory~~ is~~being~~ shared by the modem and by the central processing unit.

23. (Currently Amended) The device of claim 22, wherein the modulator/demodulator (modem) includes a second master controller, and the shared memory and the second master controller are operatively connected to each other via a second packet bus having:

control lines for conveying control signals; and

N bidirectional data lines for conveying a command packet and for conveying data packets. ~~the shared memory is an SDRAM.~~

24. (Currently Amended) The device of claim 21, wherein the plurality of peripherals additionally includes at least one of an image capture module, a display, and a flash memory.

25. (Currently Amended) The device of claim 21, wherein the first master controller controls the plurality of peripherals by issuing a ~~packetized~~ command packet commonly receivable by the plurality of peripherals over the N bidirectional data lines of the ~~common~~ packet bus~~, wherein the packetized command includes a module device select signal used for selecting one of the peripherals~~.

26. (Currently Amended) The device of claim 25, wherein the selected one of the peripherals returns a signal to the master controller to acknowledge receipt of the ~~packetized~~ command packet.

27. (Currently Amended) The device of claim 25, wherein the ~~packetized~~ command packet includes:

a field specifying a Read Transfer or a Write Transfer;

a field that specifies the length of a data packet; and

a field that indicates the start address of the requested transfer.

~~a read/write command to the memory shared by the modem and by the central processing unit.~~

28. (Currently Amended) The device of claim 27, wherein the command packet includes a module device select signal used for selecting one of the peripherals ~~wherein data read from the shared memory is sent to the central processing unit with a strobe signal, the strobe signal is used for strobing the data read into a register in the master controller~~.

29. (Currently Amended) The device of claim 23, wherein the shared memory is an SDRAM that includes a plurality of data banks and a first~~n~~ interface for interfacing the first master controller via the N bidirectional data lines of the first packet bus, and a second interface for interfacing the second master controller in the modulator/demodulator via the N bidirectional data lines of the second packet bus.

30. (Currently Amended) The device of claim 23, wherein N is four ~~the SDRAM includes a protection circuit for receiving address data from the central processing unit and the modem and for generating a protect signal upon simultaneously receiving the same address from the modem and the central processing unit~~.

31. (Currently Amended) ~~An application processor (AP) for use in a~~ communication device~~, the application processor comprises~~comprising:

a central processing unit, operatively connected to a processor bus including A address lines and M data lines, for processing data received from a plurality of peripherals, wherein the A address lines convey A bits of an address in parallel and the M data lines convey M bits of data in parallel; and

a first master controller operatively connected to the processor bus ~~including address lines~~ and to a first packet bus having N data lines ~~and to a second packet bus,~~ for controlling via the first packet bus the plurality of peripherals;~~,~~

a second master controller operatively connected to the processor bus and to a second packet bus having N data lines, ~~and~~ for controlling the signal modulator/demodulator (modem) via the second packet bus;

wherein each of the first packet bus and second packet bus includes:

control lines for conveying control signals; and

N bidirectional data lines for conveying a command packet and for conveying data packets including the M bits of data, wherein each of A and M is greater than N, and wherein A, M and N are integers.

32. (Currently Amended) The device of claim 31, further ~~including~~ comprising a memory shared by the modem and by the central processing unit, the memory being on the second packet bus.

33. (Currently Amended) The device of claim 32, wherein the shared memory is an SDRAM that includes a plurality of data banks and a first interface for interfacing the second master controller via the N bidirectional data lines of the second packet bus, and a second interface for interfacing a third master controller in the modulator/demodulator via the N bidirectional data lines of a third packet bus.

34. (Currently Amended) The device of claim 31, wherein the plurality of peripherals ~~operatively connected to~~on the first packet bus include at least one of an image capture module, a display, and a flash memory.

35. (Currently Amended) The device of claim 31, wherein the first master controller controls the plurality of peripherals on the first packet bus by issuing a ~~packetized~~ command packet commonly receivable by the plurality of peripherals over the first packet bus, the ~~packetized~~ command packet includes a module device select signal ~~used~~ for selecting one of the peripherals.

36. (Currently Amended) The device of claim 35, wherein the selected one of the peripherals returns a signal to the master controller to acknowledge receipt of the ~~packetized~~ command packet.

37. (Currently Amended) The device of claim 35, wherein the ~~packetized~~ command packet includes a read/write command directed to a memory shared by the modem and the central processing unit.

38. (Currently Amended) The device of claim 37, wherein the command packet further includes:

a field that specifies the length of a data packet; and

a field that indicates the start address of the requested transfer.

~~data read from the shared memory is sent to the central processing unit with a strobe signal, the strobe signal is used for strobing the data read into a register in the master controller.~~

39. (Currently Amended) The device of claim 33, wherein the control lines of the first

packet bus include: ~~the SDRAM includes a plurality of data banks and an interface for interfacing the master controller via the second packet bus.~~

a signal line that indicates whether the N bidirectional data lines currently carry a command packet or a data packet;

a signal line that indicates the current transfer direction over the N bidirectional data lines.

40. (Currently Amended) A method of controlling a communication device having a signal modulator/demodulator (modem) for effecting radio communications and a central processing unit, and a master controller, comprising:

controlling the~~a~~ master controller via a processor bus having A address lines and M data lines of a processor bus, wherein the A address lines convey A bits of an address in parallel and the M data lines convey M bits of data in parallel;

using the master controller to control~~ling~~ a plurality of peripherals including the signal modulator/demodulator by issuing command packets via a packet bus operatively connected to the master controller and to each of the plurality of peripherals, wherein the packet bus is characterized by having: ~~-~~

control lines for conveying control signals; and

N bidirectional data lines for conveying the command packet and for conveying a data packet including the M bits of data, wherein each of A and M is greater than N, and wherein A, M and N are integers.

41. (Currently Amended) The method of claim 40, wherein the step of controlling the signal modulator/demodulator via the packet bus includes issuing a command packet receivable at an interface of~~ing~~ a memory shared by the modem and the central processing unit.

42. (Currently Amended) The method of claim 40, wherein the shared memory is an

SDRAM, that includes a plurality of data banks and a first interface for interfacing the master controller via the N bidirectional data lines of the packet bus, and a second interface for interfacing a second master controller in the modulator/demodulator via the N bidirectional data lines of a second packet bus.

43. (Currently Amended) The method of claim 40, wherein the plurality of peripheralsstep of controlling includes controlling at least one of an image capture module, a display, and a flash memory.

44. (Currently Amended) The method of claim 40, wherein the step of controlling the plurality of peripherals includes issuing a packetized command packet commonly receivable by the plurality of peripherals over the packetcommon bus, wherein the packetized command packet includes a module device select signal used for selecting one of the peripherals.

45. (Currently Amended) The method of claim 44, wherein the selected one of the peripherals returns a signal to the master controller to acknowledge receipt of the packetized command packet.

46. (Currently Amended) The method of claim 40, wherein the packetized command packet includes a read/write command directed to a memory shared by the modem and the central processing unit.

47. (Currently Amended) The method of claim 4046, wherein data read from the shared memory is sent transmitted to the central processing unit with a strobe signal, the strobe signal is used for strobing the data read into a register in the master controller.

48. (Currently Amended) The method of claim 41, further including receiving address

~~data from the central processing unit and the modem at the shared memory and~~ generating a protect signal upon simultaneously receiving the same address in a command packet from the modem's master controller and in a command packet from the central processing unit's master controller, wherein the protect signal is generated to halt memory access by one of the signal modulator/demodulator and the central processing unit in order to prevent simultaneous access of the same memory cells by both of the signal modulator/demodulator and the central processing unit.

49. (New) The communication device of claim 11 wherein the second master controller is in the modulator/demodulator.

50. (New) The communication device of claim 11 wherein both the first master controller and the second master controller are electrically connected to the A address lines and M data lines of the processor bus.